PATENT

Appl. No. 09/659,398
Amdt. Dated August 5, 2003
Reply to Office action of May 9, 2003

REMARKS

The Examiner is thanked for the indication of allowable subject matter of claims 10-13.

The Applicants respectfully request the Examiner to reconsider the rejection of the remaining claims.

The Examiner has rejected the remaining claims, claims 1-9 and 14-20 as being obvious over the Hideharu reference, either alone or in combination with other references.

The cited references fail to establish a prima facie case of obviousness with respect to these claims. When examining a claim for obviousness, each and every limitation of the claim must be considered. A failure to consider just one claim limitation is a failure to consider the claim as a whole. 35 U.S.C. § 103 states:

> "a patent may not be obtained though the invention is not identically disclosed or described as set forth in §102 of this title, if the differences between the subject matter sought to be patented and the prior art ***are such that the subject matter as a whole*** would have been obvious....."
> (emphasis added).

The Hideharu reference does not establish a prima facie case of obviousness with respect to claim 1 because it does not teach several limitations of claim 1. A complete translation of the Hideharu reference was not provided with the Office action. Consequently, the untranslated portions of the reference cannot be cited. The only English portion of the reference does not contain any teaching of the claim 1 limitations as follows:

> "a monitoring microprocessor ***having an assurance characteristic which is higher and having a performance characteristic which is lower*** than said general purpose microprocessor,..."

There is nothing in the translated portion of the Hideharu reference which teaches this limitation. It is improper for the Examiner to claim that this is an obvious variation because the Examiner makes no reference to any of the cited references where there is even a suggestion of the desirability of having such a relationship between the monitoring microprocessor and the general purpose microprocessor. This limitation is a key aspect of the present invention, and it must not be overlooked.

Without a teaching of the limitation, and without even a mere suggestion of the desirability of such a limitation, by any of the cited references, no prima facie case of obviousness exists.

Moreover, claim 1 goes on to further limit the invention to exclude monitoring which involves real-time comparisons of parallel computations made on parallel microprocessors.

With respect to claim 14, it contains a limitation to a means for enhancing ***an integrity characteristic*** of a means for executing where the means for enhancing is further limited to exclude means which involve comparing outputs of parallel computing machines. The Applicants do not see, and the Examiner did not cite or even assert, that any portion of the Hideharu reference is a means for ***enhancing an integrity characteristic*** which ***does not involve real-time comparisons of parallel computations made on parallel microprocessors.*** Since the Examiner has failed to consider these limitations, and fails to even assert that the prior art references teach these limitations (which they do not), the Examiner has failed to establish a prima facie case of obviousness with respect to claims 14-17.

With respect to claim 18, it has been amended to even further narrow the claimed invention. In claim 18, as amended, the output of the first microprocessor is not a failure status of said first microprocessor. Since the Hideharu reference fails to teach monitoring for a non-failure status, then it does not establish a prima facie case of obviousness with respect to claims 18-20.

In general, the Applicants believe that the Examiner is relying upon the Hidedaru reference far more than can be justified based upon the limited translation available.

PATENT

Appl. No. 09/659,398
Amdt. Dated August 5, 2003
Reply to Office action of May 9, 2003

In summary, the Hideharu reference simply does not teach enhancing the integrity of a computing system. The Examiner needs to be mindful that enhancing the integrity of a computing system is not synonymous with a dual redundant system as taught by Hideharu. In Hideharu, if one processor fails, the total failure is detected and another takes over. There is no teaching that one of the processors has a higher integrity characteristic than the other. Again, this is a key aspect of the present invention. Since there is no teaching or even a suggestion of the desirability of employing two processors which enhance integrity and which have the relationships with respect to each other vis-a-vis their integrity and performance, there is no prima facie case of obviousness.

The Applicants believe that the application, as amended, is now in condition for allowance, and early notification of the same would be greatly appreciated.

Respectfully submitted,

By: _____

Kyle Eppele
Reg. No. 34,155
Attorney for Applicant

Rockwell Collins Inc.
Intellectual Property Department
400 Collins Road NE M/S 124-323
Cedar Rapids, IA 52498
Telephone: (319) 295-8280
Facsimile No. (319) 295-8777
Customer No.: 26383